

An Overview of Josephson Packaging

An overall packaging philosophy for high-speed Josephson computers is outlined in this paper. The unique characteristics of such a package, operating at liquid helium temperature, are described, and a description is given of the technologies needed to build the package.

Introduction

Even with the highest-speed integrated circuit chips, a high-speed computer cannot be realized unless a suitable package is available to support the chips. In the design of such a package, whether for room-temperature technologies or for Josephson technology, many sometimes conflicting requirements have to be met. These requirements concern mechanical, thermal, electrical, and material characteristics.

A first order requirement is that the circuit chips be interconnected with lines that limit time delay from chip to chip. Also, the pulses propagated on the lines should not be distorted significantly due to losses in the lines or by noise associated with the lines and the physical discontinuities in the package. Time delay can be limited by packaging the chips closely together and using insulators in the lines with low dielectric constants.

From a mechanical viewpoint, the chips must be held securely to the package and the different parts of the package held together correctly as the machine undergoes shifts between room and operating temperature. Mechanical designs should allow for the replacement of parts of the machine to facilitate engineering changes or to repair faulty parts. Thus, the design must include a pluggable, electrical contact, large enough to allow replacement of parts reliably and at the same time small enough to not cause excessive reflections and crosstalk as the electrical pulse passes through it.

Thermal designs have to take into account how to cool the circuit chips so that they operate at a prescribed temperature and so that variations in this temperature

throughout the system are not excessive. As the circuit count of machines increases, the problems of how to dissipate all the power produced by the circuits to the outside also has to be addressed carefully.

The process flow and the materials used in a package have to be carefully chosen to allow for compatibility, high-yield fabrication, and reliability during operation. Stress levels in the materials used, caused by the intrinsic properties of materials or by thermal cycling, should be low enough so that the mechanical properties of the package are preserved.

The Josephson computer with its package and chips will be operated near 4 K in a liquid helium environment. Advantages as well as some disadvantages result from operating at this temperature. The strip lines interconnecting the chips can be made to be superconducting (both the line and ground plane), which eliminates resistance losses that distort and attenuate high-speed pulses traveling down nonsuperconducting lines. The superconducting lines also can be made narrower, because of the lack of loss, and this allows the lines to be placed closer together, permitting the circuit packing density to be increased. Thermally activated processes that can lead to reliability problems in the package and chips are greatly reduced at 4 K. Of course, reliability problems associated with thermal stresses in the materials still have to be considered.

The provision of a liquid helium environment requires a cryocooler and dewar arrangement. Advances in the design of such equipment suggest that these can be obtained

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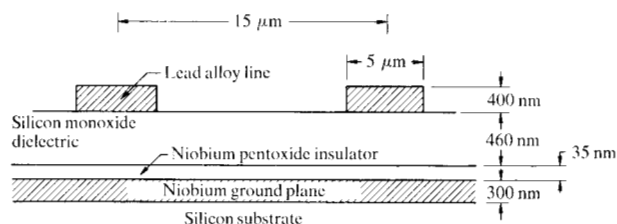


Figure 1 Strip line configuration.

at reasonable cost and provide good reliability characteristics for medium and large machines using Josephson technology. For a large machine, suitable for speeds in the range of 7×10^7 instructions per second (70 MIPS), the total heat load at 4 K would be of the order of 8.5 W; this would include heat leaking through the dewar walls and down the I/O leads, as well as that generated by the memory and logic circuits. Approximately 13 kW of unregulated power would be needed for the compressor that drives the cryocooler.

Unique characteristic of a Josephson package

In order to reduce the time of flight of signals through a package, it is obvious that the volumetric circuit packing density has to be increased. This can be done as long as there is space left in the package to allow heat to be extracted, there is room enough to place all the interconnecting lines, and control can be maintained over all the microfabrication steps needed to build up the package and bond its parts together.

Because Josephson circuits dissipate so little power, the heat flux flowing out of the back of a Josephson LSI chip is so low that it can be cooled by direct contact with naturally convected helium fluid, with the temperature drop at the interface still kept well within the limits needed by the circuit. This means that no bulky heat sinks are needed for the chip, allowing the chips to be placed closer together. Typical numbers for 1000 logic circuits on a 6.4×6.4 -mm circuit chip, including ancillary circuits, are a heat flux of 12 mW/cm² and a temperature drop of approximately 0.1 K across the chip-helium interface.

This power density is only 2 to 3 percent of that required to cause peak nucleate boiling and then thermal runaway. In contrast, cooling for high-performance semiconductor technology requires bulky heat-sink arrangements to avoid this runaway value, which is in the range of 20 W/cm² when using practical fluorocarbon coolants.

The configuration of the package to be used with the Josephson circuit is three-dimensional, having the form of cards, carrying circuit chips, plugging into a board with a gap of about 0.3 cm between the cards [1]. For this gap value the temperature drop at the chip on one card will not be affected by the presence of other cards. So the cooling of a whole package can be accomplished by placing it in the liquid He bath, orientated so that natural convection can take place; no volume has to be taken up by heat sinks.

As mentioned previously, another unique feature of the Josephson technology is that it can use superconducting lines between the chips. This allows the cross section of the line to be very small, so that both the metal thickness and linewidth can also be small. The former allows for easier formation of the line by photoresist techniques. The circuits operate into lines with impedances in the 10-ohm range, which means that the line is placed close to the ground plane, reducing the fringing fields that lead to line-to-line coupling.

A typical line configuration is shown in Fig. 1. The minimum thickness of both the line and the ground plane is set by the penetration depth of the field into the superconducting metals. The layer of Nb₂O₅ is chosen so that it will seal the ground plane from possible shorts through the SiO, while at the same time it can be thin enough in comparison with the SiO so that the velocity of propagation is set by the SiO rather than the high dielectric constant Nb₂O₅. The thickness to width ratio of the lines (1:12.5) allows the shapes to be well controlled during the photoresist stage, permitting the characteristic impedances of the line, on different members of the package, to be well matched. Hence, the narrow lines can be placed closer together, and the amount of surface in the package needed to carry the lines is greatly reduced compared to that required by room-temperature technologies.

It can be seen that out of the three general problems that any package has to meet—providing cooling paths, producing high-quality electrical lines, and the large problem of controlling the fabrication of microstructure parts—the one that must be solved for the Josephson technology is the microstructure one; the other two are much easier to deal with than is the case for room-temperature technology.

General concepts for a Josephson package

In this section we describe the packaging concepts and dimensions needed to fabricate a 70-MIPS computer. At the module level it is estimated that a density of 5000 logic circuits per cubic centimeter is needed for this speed.

In order to limit the length of lines over which signals travel in the package, a three-dimensional package was designed using a card-on-board approach [2].

The central element of the package, into which all other parts are plugged, is the board (Fig. 2). It contains a matrix of cavities set on 0.3-mm centers. Entrapped in the cavities by surface tension are balls of mercury. Modules are plugged into both sides of the board using pins attached to the wiring on the module. Pin-to-pin electrical contact is made via the mercury ball.

The modules plugged in on top are circuit modules, and those plugged in from the bottom are called wiring modules. The wiring modules have two levels of strip lines on them as well as pins to make contact with the board. The strip lines allow circuit modules to be interconnected. The circuit modules on the top of the board not only interconnect circuit chips but allow one wiring module to be stitched to the next one, via the horizontal portion of the circuit module, so that a continuous wiring pattern can be produced while using parts smaller than the board. This arrangement is necessary to accommodate wiring modifications due to engineering changes or fabrication defects. Instead of taking out the complete circuit-module-to-circuit-module wiring on one large wiring module, only small portions of it have to be removed by taking one small module out of a set of them.

The circuit module is made up of a chip carrier, two feet (one on each side of the carrier), and pins attached to the feet which then plug into the board. The chip carrier is populated by four circuit chips on each side for logic and eight for memory, and it contains strip lines to interconnect the eight or sixteen chips and also to connect a chip to pins on the foot. A pin leads to another chip on another circuit module. Small vias, cut into the silicon circuit carrier and then plated, are used to interconnect the chips that are placed on opposite sides of the carrier. The circuit modules are at right angles to the board, and compared to a topology that has the chips parallel to the board it allows more circuit chips to be supported per unit area of the board. The lines coming down vertically on the chip carrier are on 0.075-mm centers, and the board cavities are made on 0.3-mm centers. The foot acts only as a space expander allowing the 0.075-mm centers to be matched to the 0.3-mm centers. The circuit chips, 6.4 mm on a side, are bonded onto the circuit module using 228 microsoldier bonds placed in a double row around the chip periphery. They are on 0.2-mm centers.

As the superconducting line transmission characteristics are excellent and the characteristic impedances throughout the package are well matched, the most signif-

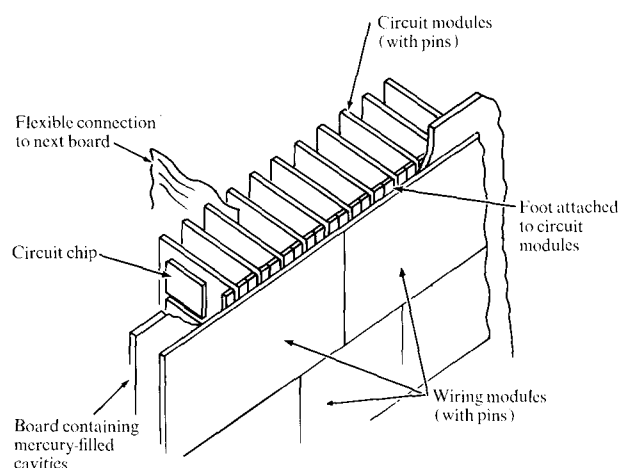


Figure 2 Board and modules configuration.

icant electrical characteristic of the package is at the package discontinuities, the circuit chip bond, the right angle bond between the circuit carrier and the foot, and the pin-mercury-pin contact [3]. These discontinuities can allow lumped inductances of up to 250 pH to appear in the lines; unless the line is formed into a low-pass filter by adding capacitors to ground at the discontinuity and the pulse is slowed, noticeable reflections would be produced in passing 30-ps pulses through them. At the same time, a degree of crosstalk is created, for instance, from one pin-mercury-pin path through the board to an adjacent one. This can be reduced by increasing the ratio of ground contacts to signal contacts at these discontinuities. This ratio is typically in the range of 1:3 to 1:8 in our present designs.

Figure 3 shows how the different populated boards can be assembled together in a box form with sufficient room inside the box for one circuit module at a time to be unplugged from the board and picked out of the assembly [4]. The natural flow of the liquid helium used for cooling would be vertical inside the box. For a 70-MIPS machine, the total machine—logic, cache, and main memory—could be contained in a volume of approximately 3400 cm³ and made up of two-board boxes. Board-to-board communication could be accomplished by flexible connections from the top of one circuit module plugged into a board to the top of another circuit module plugged into another board. The connection could be made of a film of flexible insulator with a ground plane on one side and etched lines on the other. Flexibility is needed to allow these interconnecting modules to be removed without disturbing either board.

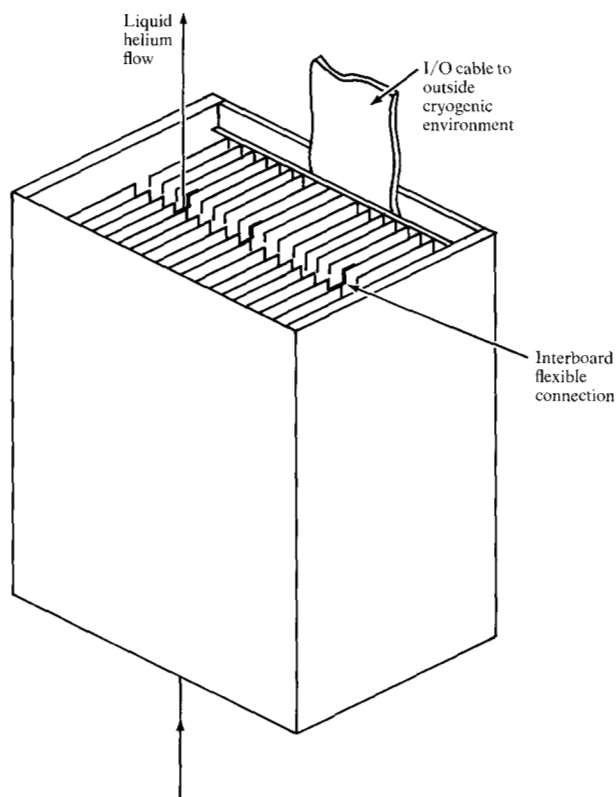


Figure 3 Populated board assembly.

Box-to-box interconnections, needed to make up a complete machine, can also be based on similar principles to those described for plugging circuit modules into the board.

Typical dimensions for the packaging parts are boards that are 6.5 cm on a side, circuit carriers that are 3 cm by 1.5 cm, connected to feet that are 3 cm long by 0.15 cm wide. The wiring modules can vary in size as called for by the design but are typically 3 cm by 1.2 cm. With such a board and using SiO as the dielectric for the strip lines, the time of flight delay from one corner of the board to the opposite one is 1150 ps.

Technologies

The technologies chosen to fabricate test vehicles for the package have been adapted from those used in making LSI circuit chips. Where this has not been possible and special techniques have had to be introduced, they have been chosen for their ability to allow batch fabrication of the part and, if possible, to have all positional accuracies set by photolithographic processing [5].

Strip lines on all packaging parts are designed so that they can employ the same thin-film and lithographic techniques used on the chip.

To limit the number of problems caused by the expansion mismatch among the packaging parts as the machine is cycled between room temperature and 4 K, one common substrate material has been used throughout. The Josephson thin-film circuits and strip lines should have a smooth and blemish-free surface on the substrate to obtain process control. Hence silicon becomes an obvious first choice for the circuit chip. Silicon is also a good choice for the board material, as microcavities can easily be anisotropically etched into it. In order to protect all the soft solder joints from excessive strain during temperature cycling, the circuit and wiring modules should also be made of silicon. At least this assures that the strain at these joints is limited to that caused by the differential expansion between the solder, the interface metallurgy, and the silicon at the joint itself. Although ceramic substrates would have been mechanically stronger, they do not fit into the overall process design.

All parts, except the pluggable connections, are bonded together using low melting point solders. The chips are bonded onto the carrier using a controlled collapse reflow micro solder technology [6]. The micro solder contacts are 0.1 mm in diameter on 0.2-mm centers. The solder and the interface metallurgy needed to provide a good bond between the Nb pad (used to end the strip lines) and the solder are formed by sputtering the interface metallurgy and evaporating the solder, both through a metal mask with its holes aligned to the pads on the chip. The solder has a melting point below 70°C which is the maximum processing temperature allowed for the chip. Using a flux that is active below 70°C, the chip is then bonded onto the carrier.

However, before this step the pins have been soldered onto the foot, using a solder with a melting point of 117°C, and the foot has been bonded onto the carrier using the same solder. The solder in this foot bond electrically connects strip lines leading from the pins on the underside of the foot to strip lines on the carrier. The solder bonds also provide the mechanical strength needed for the circuit module both during fabrication and subsequent cycling from room temperature to 4 K. To increase this strength similar bonds are produced on the top side of the foot, but in this case they do not provide electrical contact.

One of the most difficult requirements when the package becomes increasingly small is to provide pluggable contacts. These contacts, mentioned previously, have been fabricated using known technologies but applied in a

novel fashion to this problem. To meet very tight positional tolerances, both the pins on the modules and the cavities in the board are formed starting with photolithographic techniques. The cavities are made by etching truncated pyramidal cavities in a silicon wafer by chemical anisotropic etching. Two such wafers are then placed back to back and bonded to form the cavities needed. The pins are formed from a solid platinum foil, using electrodischarge machining techniques. A tool for this operation is formed from a thin molybdenum sheet with holes chemically etched in it using photolithographic techniques. This tool, under servo control, is driven down onto the platinum; by producing electrical discharges between the two pieces, small 0.075-mm-diameter pins are formed wherever a hole is present in the tool. (The pin length is 0.2 mm.) In this fashion an array of pins is formed that, after a transfer technique, is bonded onto the various modules employed in the package, keeping pin and socket positional tolerances under tight control throughout. The via holes needed on the chip carrier have been cut using portions of this same technique. When the array of pins has been cut by the machine's molybdenum mask, in this case from a copper block, the pin set is used to cut the vias in the silicon circuit carrier. The correct doping level has to be chosen to allow conduction during machining but to have perfect insulation at 4 K.

The circuit module shown in Fig. 4 was part of a test vehicle to develop the packaging technologies. A single chip mounted in the middle of the circuit carrier uses the microsolder technology. The lower row of pads on the circuit carrier are shown bonded to a similar row of pads on the underside of the foot. Also bonded on the foot is the array of 0.075-mm-diameter pins that make contact with the mercury balls in the board. Heads were cut into the pins by using a different size hole in the metal mask from that used for cutting the pin shanks. The head allows stronger pin bonds to be made. The larger pins visible at the ends of the foot are used to guide the circuit module into the board without harming the small pins. In this particular vehicle the bonds joining the strip lines on the carrier to those on the foot are on 0.15-mm centers, the cavities are on 0.5-mm centers, and the microsolder bonds on the chip, 84 in number, are placed on 0.2-mm centers.

The pin centers and foot-carrier bond centers have to be reduced by approximately a factor of two and the mi-

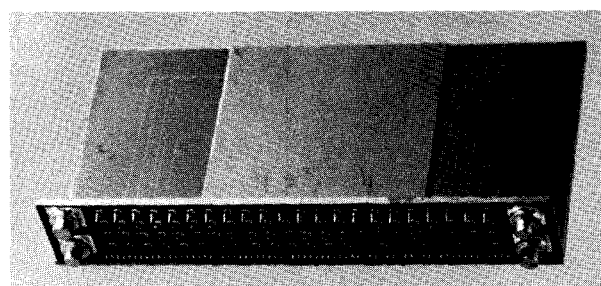


Figure 4 A test circuit module.

crossolder bond count on the chips has to be increased by approximately a factor of three to allow these technologies to be used in the fabrication of a 70-MIPS machine.

Conclusions

Because of the Josephson circuit's low power dissipation and because superconducting lines are used for interconnection in the package, the Josephson technology provides two very important advantages for the package. It does not need bulky and complex cooling structures to get the heat out of the chips, and the quality of signal transmission across the package is greatly enhanced due to the lack of electrical loss in the superconducting lines. However, achieving the fabrication controls necessary to make the required microstructures for a 70-MIPS machine remains to be done.

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